

DO NOT ENTER: /E.M./

**EXPEDITED PROCEDURE
AFTER FINAL REJECTION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Walter Fix et al.
Serial No.: 10/562,869
Filed: April 7, 2006
For: Logic Gate with a Potential-Free Gate Electrode for Organic Integrated Circuits
Examiner: Eva Y. Montalvo Art Unit: 2814
Attorney Dkt: 411000-144 Customer No. 27162

AMENDMENT UNDER 37 CFR 1.116

MS AF
Commissioner for Patents
Box 1450
Alexandria, VA 22313-1450

This paper is in response to the final Office Action dated July 16, 2010 having due date for response set to expire on October 18, 2010. While no fee is believed due for this paper, the Commissioner is authorized to charge deposit account 03 0678 for any fee that might be due for this paper or credit any over payments to this account.

IN THE TITLE

Amend the title to read as follows:

- - Logic Gate having a Transistor Gate Capacitively Coupled to the Transistor's Source or Drain Electrode- -

IN THE DRAWING

Amend the drawing to add new figures 5 and 6 as shown in the attached new sheet of drawing.

IN THE SPECIFICATION

Amend the specification as shown on page 2 of this paper.

Remarks begin on page 3.